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Docket No.: 0057-2362-2YY

COMMISSIONER FOR PATENTS
ALEXANDRIA, VIRGINIA 22313

Re: Group Art Unit: 2811
Serial No.: 09/176,315
Filed: OCTOBER 22, 1998
Applicant: SHIGENOBU MAEDA, ET AL
For: METHOD OF DESIGNING SEMICONDUCTOR DEVICE, SEMICONDUCTOR DEVICE AND...

Attached hereto for filing are the following papers:

<u>APPEAL BRIEF, APPENDIX, ATTACHMENT (in triplicate)</u>

Please note that this is the <u>second Appeal Brief</u> applied for this application. No fees are required. In the event any variance exists between the amount enclosed and the Patent Office charges for filing the above-noted documents, including any fees required under 37 C.F.R. 1.136 for any necessary Extension of Time to make the filing of the attached documents timely, please charge or credit the difference to our Deposit Account No. 15-0030. Further, if these papers are not considered timely filed, then a petition is hereby made under 37 C.F.R. 1.136 for the necessary extension of time. A duplicate of this sheet is enclosed.

Respectfully submitted,

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IN THE UNITED STATES PATENT & TRADEMARK OFFICE

IN RE APPLICATION OF:	:
SHIGENOBU MAEDA ET AL.	: EXAMINER: CRANE, S.
SERIAL NO: 09/176,315	:
FILED: OCTOBER 22, 1998	: GROUP ART UNIT: 2811

FOR: METHOD OF DESIGNING SEMICONDUCTOR DEVICE, SEMICONDUCTOR DEVICE AND RECORDING MEDIUM

APPEAL BRIEF

COMMISSIONER FOR PATENTS
ALEXANDRIA, VIRGINIA 22313

SIR:

This is an appeal of the most recent Final Rejected dated January 14, 2003, of Claims 1-5 and 18 that is hereinafter referred to as FR. A Notice of Appeal from this FR was timely filed on June 16, 2003.

I. REAL PARTY IN INTEREST

The real party in interest in this appeal is Mitsubishi Denki Kabushiki Kaisha having a place of business at 2-3 Marunouchi 2-chome, Chiyoda-ky, Tokyo 100-8310, JAPAN.

II. RELATED APPEALS AND INTERFERENCES

Appellants, Appellants' legal representative, and the assignees are aware of no appeals which will directly affect or be directly affected by or have a bearing on the Board's decision in this appeal.

III. STATUS OF CLAIMS

Claim 1-5 and 18 stand finally rejected, which forms the basis for this appeal. Claims 6-16 and 19 have been rewritten to be in independent form by the Amendment filed June 16, 2003. The Advisory Action of July 14, 2003, indicates that these claims have been allowed. Claims 17 and 20, the only other claims remaining in this application, have been withdrawn from consideration by the Examiner as being to species that were non-elected with traverse.

IV. STATUS OF THE AMENDMENTS

As noted above, the amendments filed after the FR on June 16, 2003, was entered. The attached Appendix I reflects the finally rejected claims that were last amended on October 5, 2000.

V. SUMMARY OF THE INVENTION

The present invention is directed to a method of determining a layout pattern for an MOS transistor and the MOS transistor resulting from using this layout pattern. This MOS transistor layout pattern is used to form an MOS transistor SOI structure like that of FIGS. 1-2, for example, and is determined based upon an operating clock frequency that is equal to or greater than 500 MHZ while still providing the MOS transistor SOI structure with stable operation. In order to provide for this highspeed and stable operation, Applicants have discovered that the layout pattern must be determined to satisfy the conditional expression $R \bullet C \bullet f < 1$, where R represents the resistance of a fixed potential transmission path extending from a body contact on a body portion of the MOS transistor to a body region that is between

a first semiconductor region of first conductivity type and a second semiconductor region also of the first conductivity type that are both formed in an SOI layer of the MOS transistor, C represents the gate capacitance of the MOS transistor, and f represents the operating frequency of a predetermined clock that is equal to or greater than 500 MHZ. The flow chart of FIG. 4, for example, summarizes the steps of the method and notes the generation of a layout pattern with a maximum allowable gate width W_{max} that is determined to satisfy this conditional expression. FIG. 5 shows an example of using a layout pattern generating device to implement the method and provide layout pattern data to be used to actually make the MOS transistor.

In another aspect of the invention, an MOS transistor having an SOI structure is formed using a layout pattern for the MOS transistor determined to satisfy the conditional expression $(R \bullet C)/td<1$. In this conditional expression, td represents signal propagation delay time (s) required for the MOS transistor that is less than 50 ps, with the parameters R and C being those noted above. This is summarized in the flow diagram of FIG. 7, for example, which notes generation of a layout pattern with the maximum allowable gate width W_{max} that is determined to satisfy this conditional expression.

VI. ISSUE

The only issue is whether or not the subject matter of Claims 1-5 and 18 would have been obvious to one or ordinary skill in the art in the sense of 35 U.S.C. §103 over Iwamatsu et al (the 1995 article entitled "*High-Speed* 0.5 μm *SOI 1/8 Frequency Divider with Body-Fixed Structure for Wide Range of Applications*) (Iwamatsu) in view of Agari (JP 6-224302),

Chen et al (U.S. Patent No. 5,767,549) (Chen), Blake et al. (U.S. Patent No. 4,899,202, Blake), Gunning (U.S. Patent No. 5,023,488), and Masuda et al (U.S. Patent No. 3,855,610, Masuda).

VII. GROUPING OF THE CLAIMS

Claims 1, 2, 5, and 18 will stand or fall separately and are argued separately below. Claim 3 will stand or fall with Claim 1 and Claim 4 will stand or fall with Claim 2.

VIII. ARGUMENT

1. The subject matter of Claims 1 and 2 has not been properly analyzed.

Turning to the outstanding final rejection of Claims 1 and 2 under 35 U.S.C. §103 as unpatentable over Iwamatsu in view of Agari, Chen, Blake, Gunning, and Masuda, it is first noted that the FR adopts the reasoning presented in the Office Action mailed on December 20, 2000, hereinafter referred to as the December 20 Action.

Accordingly, these arguments based upon only Iwamatsu, Agari, and Chen are addressed as they were in the first Appeal Brief filed on February 5, 2002 in terms of noting that the December 20 Action incorrectly suggests that Iwamatsu "teaches each of the structural elements of Claims 1 and 2" while ignoring that the subject matter of Claims 1 and 2 actually recites methods of designing a semiconductor device including a MOS transistor, where each of these claims require a different manner of determining a layout pattern for the MOS transistor.

The layout pattern of Claim 1 must be determined based on the operating frequency of a predetermined clock that must have a frequency "f" greater than or equal to 500 MHZ while the layout pattern of Claim 2 must be determined based on a signal propagation delay time "td" required for the MOS transistor that is less than 50 ps.

Claim 1 further requires the meeting of a specific conditional expression "R•C•f<1," with "f" being greater than 500 MHZ, with R being the resistance of a fixed potential transmission path extending from a body contact on a body portion of the MOS transistor to a body region that is between a first semiconductor region of first conductivity type and a second semiconductor region also of the first conductivity type, with the first and second semiconductor regions both being in an SOI layer of the MOS transistor, and C being the gate capacitance of the MOS transistor. Claim 2 further requires the meeting of a specific conditional expression "(R•C)/td<1," with "td," "R," and "C" as defined above.

As has been noted time and again throughout the prosecution of this application, Agari only teaches designing a semiconductor device in a manner minimizing RC delay from the resistance value and the capacitance value of each wiring part using a wiring layout and Chen only teaches controlling doping of the body of an SOI device so that the RC time constant in the body link or recessed region 20 defined by Chen to be from a respective channel to the substrate contact 39 can be as short as or less than 1 nsec. As those of ordinary skill would understand, a wiring layout is not a layout pattern of an MOS transistor and doping is not a step of providing an operating frequency of a predetermined clock, much less a step of determining a layout pattern of an MOS transistor based on the operating frequency of such a provided predetermined clock limitations that Claim 1 recites. Thus, even if the

teachings of Agari and Chen are in some reasonable manner combined with Iwamatsu, the result would not be the subject matter of Claim 1.

In response to these points raised in the first Brief, the Examiner reopened prosecution with the new first Office Action mailed May 24, 2002, that modified the rejection by adding Blake, Gunning, and Matsuda. These newly added references were indicated to be relied upon as sources of definitions and teachings of what was previously alleged to be "well-known to one having ordinary skill in the art." Applicant responded to the new first Office Action in a Request for Reconsideration filed October 21, 2002, by pointing out that the evidence offered to support the assertion of these teachings being "well-known" was not the kind of evidence of "well-known"status required to be presented by In re Ahlert, 165 USPQ 418, 421 (CCPA 1970). In this regard, Ahlert states that "assertions of technical facts in areas of esoteric technology must always be supported by citation of some reference work" (emphasis added). Patents are clearly not reference works. Moreover, patents, have been held to not be weighty evidence of wide spread recognition. See In re Barr, 170 USPQ 330, 334-34 (CCPA 1971) ("[W]e agree with the solicitor that these patents are not weighty evidence of art recognition ...").

This response of October 21, 2003, then pointed out that even if the teachings of Blake, Gunning, and Masuda are considered along with the actual teachings of Iwamatsu, Agari, and Chen, the result of that consideration would not be the subject matter of Claims 1-5 and 18 as follows:

> Turning to the reasoning for the rejection presented in the December 20 Action, the reliance stated at page 2 thereof as to Chen is with regard to col. 7, lines 29-34 which is misstated to teach the doping of "the body of an SOI MOS transistor [to] minimize the RC time constant due to the body link."

What col. 7, lines 29-34 actually teach is controlling the RC time constant "in the body link or recessed region 20 from a respective channel to substrate contact 39" by providing an "appropriate doping concentration in recessed region 20." No doping of the body of any SOI MOS transistor is taught "[to] minimize the RC time constant due to the body link" as erroneously stated here.

Moreover, while Chen further states (at col. 3, lines 19-22) that field effect transistors 26 formed on the mesas 24 have a "body" and that these "bodies of field effect transistors 26 are in ohmic contact due to recessed region 20 of silicon layer 18," this has no relevance to doping the "body link or recessed region 20" that extends from "a respective channel" of each transistor to the "substrate contact 39."

Moreover, as Chen already defines the body of each of these field effect transistors 26 to be apart from recessed region 20 that then serves to "link" (hence the name "body link") each of these bodies of field effect transistors 26 to substrate contact 39, the reason why the artisan would look to Blake to define a transistor body is not set forth in violation of recent precedent. See In re Rouffet, 47 USPQ2d, 1453, 1459 [(Fed. Cir. 1998)] requiring the PTO to "explain the reasons one of ordinary skill in the art would have been motivated to select the references and to combine them to render the claimed invention obvious." [Emphasis added.]

Furthermore, whatever Blake defines to be a "body node" (at col. 1, lines 55-58) in terms of an "undepleted volume within the body region underlying the gate electrode," in no way modifies the teachings of Chen that there is a "body link, or recessed region 20 from a respective channel to substrate contact 39" that is separate from the "bodies" of transistors 26 as Chen uses these terms. Clearly, each transistor "body" 26 of Chen is not the same thing as the "body link" that is equated by Chen to the recessed region 20 at col. 7, line 3.

Furthermore, page 2 of the outstanding Action errs in suggesting that the word "body" can be taken out of context from the other teachings of Chen. Such an approach is prohibited by the PTO reviewing Court in In re Kotzab, 55 USPQ2d 1313, 1317 (Fed. Cir. 2000) as follows:

> While the test for establishing an implicit teaching, motivation, or suggestion is what the ... statements of [the reference] would have suggested to those of ordinary skill in the art, the [reference] would have suggested to those of ordinary skill in the art, the [reference] statements cannot be viewed in the abstract. Rather, they must be

considered in the context of the teaching of the entire reference. [Emphasis added.]

In addition, the teachings of Blake at col. 1, lines 55-68 and col. 5, lines 23, 33, 37, and 53-60, all noted as being relied upon in the outstanding Action, make it clear that the "body node," the "undepleted volume under the gate electrode," "is below the channel of transistor 100 when conducting," see Blake at col. 5, lines 59-60. This means that Blake teaches the body node is actually more distant from any gate electrode and gate electrode capacitance than immediately below the channel. See the "depletion regions" of Figs. 35 and 36 from pages 203 and 204 of Sze, SEMICONDUCTOR DEVICES, Physics and Technology, 1985, attached hereto. Just as gate capacitance between a gate and the substrate surface it is separated from by a gate oxide is not a capacitance "in the body link or recessed region 20" of Chen, it is also not a capacitance in the body node of Blake.

Clearly, those skilled in the art would have no reason to believe that the "body link" of Chen relates to the channel 32 illustrated in Fig. 1 of Chen or anything illustrated to be above that channel such as the Fig. 1 illustrated gate 27 above the gate oxide 34 that is above each channel 32, see col. 3, lines 15-18 of Chen. Thus, the "C" of concern to Chen as to the col. 7, lines 29-34 teaching of controlling the "RC" time constant "in the body link or recessed region 20 from a respective channel to substrate contact 39" (emphasis added) precludes any consideration of gate capacitance relative to the Fig. 1 illustrated gate 27 above the gate oxide 34 that is above each channel 32, at least to those familiar with the clear meaning of the words used by Chen.

Thus, applicants do not argue that the prior art does not recognize the existence of gate capacitance as alleged at page 3 of the outstanding Action; instead, the argument is clear that whatever the "C" of concern to Chen as to the col. 7, lines 29-34 teaching of controlling the "RC" time constant "in the body link or recessed region 20 from a respective channel to substrate contact 39" (emphasis added) might be, it cannot be **REASONABLY** said to be gate capacitance between the surface above channel 32 separated from gate 27 by gate oxide 34, as none of these elements are "in the body link or recessed region 20 from a respective channel to substrate contact 39" (emphasis added). As noted above, just as gate capacitance between a gate and the substrate surface it is separated from by a gate oxide is not a capacitance "in the body link or recessed region 20" of Chen, it is also not a capacitance in the body node of Blake.

The argument of the [first] Appeal Brief at page 11-12 pointing out true sources of "C" "in the body link or recessed region 20 from a respective channel to substrate contact 39" (emphasis added) was just that, not a denial

> that gate capacitance does not exist **ELSEWHERE**. This argument remains relevant as the mere indication by Gunning of "drain-side capacitances," "source-side capacitances" and "gate-substrate capacitance" and that of Masuda as to "C_{GP}," "C_{GS}," and C_{PS}," do not change the simple fact that the "C" of concern to Chen as to the col. 7, lines 29-34 teaching of controlling the "RC" time constant "in the body link or recessed region 20 from a respective channel to substrate contact 39" (emphasis added).

The first Appeal Brief further pointed out that with regard to Claim 2, the steps of providing a signal propagation delay time that is less than 50 ps for a MOS transistor and then determining a layout pattern of this MOS transistor based on this signal propagation delay time was also clearly not taught by Agari or Chen. Thus, even if the teachings of Agari and Chen were, in some reasonable manner, combined with Iwamatsu, the result would not be the subject matter of Claim 2. Again, the addition of Blake, Gunning and Matsuda does not change this statement.

Moreover, even as to semiconductor devices of Claims 3 and 4, the criticality of the layout patterns being appropriately determined cannot be dismissed in terms of the structural relationships that still must exist in the manufactured semiconductor device in terms of the above-noted parameters of "R" and "C" having values that taken with a frequency "f," having a value greater than 500 MHZ, will satisfy the conditional expression "R•C•f<1" and that taken with a propagation delay time "td," having a value that is less than 50 ps, will satisfy the conditional expression "(R•C)/td<1."

As has been repeatedly noted during prosecution of this application, proper and reasonable interpretations of claim limitations are required if the PTO is to perform its well established duty of properly analyzing the differences between the claimed subject matter and the prior art. See In re Dembicziak, 50 USPQ2d 1614, 1616 (Fed. Cir. 1999) as follows:

> A claimed invention is unpatentable if the differences between it and the prior art "are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art." 35 U.S.C. §103(a) (Supp. 1998); *See Graham v. John Deere Co.*, 383 U.S. 1, 14, 148 USPQ 459, 465 (1966). The ultimate determination of whether an invention is or is not obvious is a legal conclusion based on underlying factual inquiries including: (1) The scope and content of the prior art; (2) the level of ordinary skill in the prior art; (3) the differences between the claimed invention and the prior art; and (4) objective evidence of nonobviousness. *See Graham*, 383 U.S. at 17-18, 148 USPQ at 467; *Miles Labs, Inc. v. Shandon, Inc.*, 997 F.2d 870, 877 27 USPQ2d 1123, 1128 (Fed. Cir. 1993).

Furthermore, Dembicziak indicates that "the Graham decision (148 USPQ at 467) requires "strict observance" of factual predicates to any determination of obviousness. However, the PTO has made no attempt to properly analyze the differences between the claimed invention and the prior art by giving reasonable meaning and effect to every limitation in independent Claims 1 and 2 at any time during the present prosecution of this application.

It is also well established that "every limitation positively recited in a claim must be given effect in order to determine what subject matter that claim defines." In re Wilder, 166 USPQ 545, 548 (CCPA 1970). Note also In re Wilson, 165 USPQ 494, 496 (CCPA 1970) ("all words in a claim must be considered in judging the patentability of that claim against the prior art").

Besides failing to properly analyze the differences between the limitations of Claims 1 and 2 the prior art and failing to properly consider all the words of these claims, the FR misinterprets the fair and reasonable teachings of Agari, and Chen, Iwamatsu, Blake, Gunning, and Matsuda.

2. Actual Reference Teachings.

The relied upon December 20 Action indicates that Agari teaches designing a semiconductor device in a manner "minimizing RC delay from the resistance value and the capacitance value of each wiring part" (emphasis added, see the bottom of page 2 of the December 20 Action). However, the relied upon December 20 Action and all subsequent Actions ignore that the teachings of Iwamatsu include the illustrated X and Y wiring lines. If the artisan is to take the teachings of Agari in proper context, as they must be taken, see, for example, In re Wasslau, 147 USPQ 391, 393 (CCPA 1965), then all that Agari can be said to reasonably teach is that a wiring layout having a capacitance "C,"as to spacings between wiring parts that have a particular resistance "R" will have an RC wiring delay. It is this RC wiring delay ("from the resistance value and the capacitance value at each wiring part" (emphasis added) that is further taught by Agari to be minimized by a wiring layout design. Clearly, this wiring layout is not the claimed layout of an MOS transistor on an SOI layer.

Accordingly, what is clearly missing from the rejection is some reasonable basis to expand the teachings of Agari from a concern with wiring spacing capacitances and associated wiring resistance having an RC delay to be minimized into a concern with the capacitance of a gate separated from a channel region by an oxide layer and the resistance of a fixed potential transmission path extending from at least one body contact to a body region of Iwamatsu. Whatever else can be said about Chen, Agari, Iwamatsu, Blake, Gunning, and/or Masuda, it cannot be reasonably said that any of them present any reason to believe that the artisan would be concerned with wiring delay other than the wiring delay relative to illustrated X and Y wiring lines of Iwamatsu, given that the above-noted teachings of Agari

clearly relate to designing a wiring mask layout for external wiring, not the layout of an MOS transistor formed on an SOI layer. In this regard, the response filed on March 20, 2001, indicated that:

> The Action appears to suggest (at the top of page 3) that Agari somehow teaches minimizes the RC time constant of a body contact because of the improperly extracted reference to a "wiring part" at the bottom of page 2 of the Action. However, it is clear that Agari actually teaches the optimizing of wiring line widths and spacings in terms of minimizing the RC delay of a "wiring part," where the term "wiring" is one the artisan would not use to describe a body contact portion. Thus, when the "PURPOSE" and all of the "CONSTITUTION" portions of the "ABSTRACT" are read together to understand what Agari is referring to as a "wiring part" and the typical use of the term "wiring" is considered, it is clear that line width and spacing are relative to standard surface wiring and this width and spacing of the "wiring part" are controlled to minimize RC delay by controlling values of resistance and capacitance corresponding thereto. In this last regard, it is well established to be "impermissible within the framework of section 103 to pick and choose from any one reference only so much of it as will support a given position, to the exclusion of other parts necessary to the full appreciation of what such reference fairly suggests to one of ordinary skill in the art" (In re Wasslau, 147 USPQ 391, 393 (CCPA 1965)).

Thus, the teachings of Agari taken in context, as they must be taken, are clearly stated to be directed determining a wiring mask layout "so that the line and space at each wiring part may be the optimum line and space calculated respectively" (emphasis added). Thus, the Examiner has misinterpreted the Agari teaching that it is time delays due to wiring parts that have lines with capacitance inducing spaces there between that are the concern. The Examiner has further improperly suggested that these clear teachings of Agari (as to planning actual wiring layout with well defined spaces and corresponding capacitance effects) would be interpreted by those of ordinary skill in the art as teachings to apply to something other than the similar surface wiring lines shown as x and y by Iwamatsu. Missing, however, is the "logical reason apparent from positive, concrete evidence of record" (In re Regel, 188 USPQ

136, 139 n.5 (CCPA 1975)) why the artisan would have been reasonably led to conclude that something other than planning the layout of wiring, like the wiring lines shown as "x" and "y" by Iwamatsu, was being suggested by Agari. Clearly, there is nothing in the wiring layout teachings of Agari that suggests anything but a wiring layout plan to optimize surface wiring like the "x" and "y" wires of Iwamatsu.

Moreover, there are clearly no teachings or suggestions any of the relied upon references to design the layout of anything to "satisfy the conditional expression R•C•f<1 where C = the gate capacitance of said MOS transistor, R= the resistance of a fixed potential transmission path extending from said at least one body contact to said body region and f = the operating frequency of said predetermined clock, and f ≥ 500 MHZ" as required by Claim 1.

Apparently realizing that the mere reference to minimizing "RC delay from the resistance value and the capacitance value at each wiring part" in the determination of "optimum line width and space at every wiring part" (see the "PURPOSE" portion of the Agari abstract) for determining a wiring mask layout teaches nothing as to satisfying the above-noted Claim 1 layout design criteria involving the capacitance of a gate electrode and the resistance of an entirely separate fixed potential transmission path, the relied upon December 20 Action looked to the Chen teaching (at col. 7, lines 29-34) for the missing logical basis to suggest that the artisan would employ the method of Claim 1 in making the semiconductor device of Iwamatsu.

However, this relied upon teaching of Chen only teaches doping the body of an SOI device so that "the RC time constant in the body link or recessed region 20 from a respective

channel to the substrate contact 39 can be as short as or less than 1 nsec." (Emphasis added.) The concern with the values of "R" and "C" in the body link or recessed region 20 could not be more clearly stated. The lack of any reasonably taught method of determining a layout pattern for an MOS transistor based on an operating frequency is also clear. The definition of this "body link or recessed region" "as being" from a respective channel to the "substrate contact" could also not be more clearly stated.

These deficiencies notwithstanding, the Examiner seeks to interpret the "body link" language of Chen as if it were an abstract term not defined by Chen. In this respect, the teachings of Chen (at col. 7, lines 29-34) have been repeatedly misstated by the Examiner as being to dope the "body of an SOI MOS transistor to minimize the RC time constant due to the body link." What col. 7, lines 29-34 actually teach is controlling the RC time constant "in the body link or recessed region 20 from a respective channel to substrate contact 39" by providing an "appropriate doping concentration in recessed region 20, emphasis added." No doping of the body of any SOI MOS transistor is taught "[to] minimize the RC time constant due to the body link" as erroneously asserted. It is clearly improper to ignore this full statement of Chen that is clearly part of the evidence of record that always must be considered in full. See In re Chu, 36 USPQ2d 1089, 1094 (Fed. Cir. 1995).

Not only was this point raised as to the actual teachings of relied on col. 7, lines 29-34 of Chen never been acknowledged or answered by the Examiner, the further arguments as to deficiencies in the interpretation being offered as to Chen have also never been acknowledged or answered. In this regard, it is again noted to be clear that while Chen further states (at col. 3, lines 19-22) that field effect transistors 26 formed on the mesas 24

have a "body" and that these "bodies of field effect transistors 26 are in ohmic contact due to recessed region 20 of silicon layer 18," this has no relevance to doping the "body link or recessed region 20" that is defined by Chen to extend from "a respective channel" of each transistor to the "substrate contact 39." Thus, it has been emphasized that Chen defines the body of each of field effect transistors 26 to be separated from recessed region 20 that then serves to "link" (hence the name "body link") each of these bodies of field effect transistors 26 to substrate contact 39. Therefore, the reason why the artisan would look to Blake to define a transistor body when there is no ambiguity in Chen is not set forth in violation of recent precedent. See again Rouffet, at 47 USPQ2d, 1459 requiring the PTO to "explain the reasons one of ordinary skill in the art would have been motivated to select the references and to combine them to render the claimed invention obvious." [Emphasis added.]

Instead of answering these specific points, the present FR simply continues the attempt to maintain reliance on misstatements of the teaching of Chen in the December 20 Action. It also improperly suggests that col. 5, lines 25-30 of Chen can be interpreted in light of only Figure 3, while ignoring the above-noted statements of Chen, as well as col. 5, lines 6-11 (that further clearly indicate that recessed region 20 and the channel region 32 under the MOSFET gate are different regions). As noted above, however, the context of reference teachings cannot be ignored.

Clearly, whatever else can be **REASONABLY** said about the above noted Chen teaching of controlling the RC time constant "in the body link or recesed 20 from a respective channel to substrate contact 39" by providing an "appropriate doping concentration in recessed region 20," it cannot be **REASONABLY** said to apply to the

channel region 32 under the gate of a transistor based on the further unreasonable interpretation that this channel region 32 is part of the "transistor body regions (underlying the gate electrodes of the transistors)" as the Examiner urges. Also, the teaching is to modify doping, it is not a teaching of any step of determining a layout pattern for an MOS transistor based on the requirements found on either Claim 1 or Claim 2.

As noted above, it is a clearly erroneous approach to ignore the actual evidence of record in terms of the exact words of Chen as to what is meant by controlling the RC time constant "in the body link or recessed region 20 from a respective channel to substrate contact 39" by providing an "appropriate doping concentration in recessed region 20" and to substitute the Examiner's augmentation of that teaching as to controlling the "total RC time constant" as at the middle of page 3 of the FR. Clearly, it is further erroneous for the PTO to augment actual reference teachings in this manner. See In re Rijckaert, 28 USPQ2d 1955, 1957 (Fed. Cir. 1993).

Further in this regard, it is believed to be clear that those skilled in the art would have no reason to believe that the "body link" of Chen relates to the channel 32 illustrated in Fig. 1 of Chen or anything illustrated to be above that channel 32 such as the Fig. 1 illustrated gate 27 above the gate oxide 34. See col. 3, lines 15-18 of Chen. Thus, whatever components the "C" of concern to Chen (as to the col. 7, lines 29-34 teaching of controlling the "RC" time constant "in the body link or recessed region 20 from a respective channel to substrate 39" (emphasis added)) might include, they cannot be **REASONABLY** said to include the capacitance above channel 32 between gate 27 and the surface of this channel

region, as none of these elements are "in the body link of recessed region 20 from a respective channel to substrate contact 39."

Furthermore, the mere indication by Gunning of "drain-side capacitances," "source-side capacitances" and "gate-substrate capacitance" and that of Masuda as to "C_{GP}," "C_{GS}," and C_{PS}," do change the simple fact that the "C" of concern to Chen as to the col. 7, lines 29-34 teaching of controlling the "RC" time constant "in the body link or recessed region 20 from a respective channel to substrate contact 39" (emphasis added) includes no such capacitance components, otherwise known or not, as noted above.

Moreover, it appears from the actual context of Chen that the "C" recited at col. 7, lines 29-33, is the junction capacitance of the background discussion at col. 1, lines 20-22, the lessening of which is said to lead to higher circuit speed. See col. 5, lines 6-11 of Chen, noting that when "silicon layer 18 is fully-depleted under drain '28' and source 30 junctions" the result is eliminating the parasitic capacitance and gaining circuit speed." Col. 5, lines 11-14 of Chen go on to note that such full-depletion may require "counter-doping by ion implantation... to make the area beneath the source and drain fully depleted." This is clearly doping providing an "appropriate doping concentration in the body link 20" that will provide further circuit speed and not connected to any determination of a layout pattern. While col. 5, lines 19-27, of Chen discusses the relationship of "sheet resistence of recessed region 20" and doping level in this recessed region 20, conspicuous by its absence is any hint of any concern with gate capacitance or the use of any capacitance in determining any MOS transistor layout plan.

In this last respect, it is burden of the PTO to demonstrate a *prima facie* case of obviousness which means the PTO must show that the relied upon references teach all of the limitations of the claims without resort to speculation to fill gaps missing from reference teachings. Note the following from In re Warner, 154 USPQ 173, 178 (CCPA 1967):

> A rejection based on section 103 clearly must rest on a factual basis, and these facts must be interpreted without hindsight reconstruction of the invention from the prior art. In making this evaluation, all facts must be considered. The Patent Office has the initial duty of supplying the factual basis for its rejection. It may not, because it may doubt that the invention is patentable, resort to speculation, unfounded assumptions or hindsight reconstruction to supply deficiencies in its factual basis. To the extent the Patent Office rulings are so supported, there is no basis for resolving doubts against their correctness. Likewise, we may not resolve doubts in favor of the Patent Office determination when there are deficiencies in the record as to the necessary factual basis supporting its legal conclusion of obviousness. [Emphasis added.]

Instead of such evidence, the Examiner seeks to ignore the actual teaching of col. 7, lines 29-34 of Chen as to of controlling the "RC" time constant "in the body link or recessed region 20 from a respective channel to substrate contact 39" (emphasis added) and to create a new teaching that Chen somehow refers to the total RC time constant. This Examiner imagined teaching is further distorted to be the "sum of all contributing RC time constants as explained in the Agari reference" (see the bottom of page 3 of the May 20, 2002, Action). As explained above, Agari is concerned with wiring delays and wiring spacing induced capacitance, not a "sum of all contributing RC time constants" as the Examiner urges.

With further regard to the above noted misinterpretation of Blake, it is again noted that whatever Blake defines to be a "body node" (at col. 1, lines 55-58) in terms of an "undepleted volume within the body region underlying the gate electrode," in no way modifies the teachings of Chen that there is a "body link, or recessed region 20 from a

respective channel to substrate contact 39" that is separate from the "bodies" of transistors 26 as Chen uses these terms. Clearly, each transistor "body" 26 of Chen is not the same thing as the "body link" that is equated by Chen to the recessed region 20 at col. 7, line 3, all as noted above.

Furthermore, the teachings of Blake (at col. 1, lines 55-68 and at col. 5, lines 23, 33, 37, and 53-60), relied upon by the Examiner, make it clear that the "body node," the "undepleted volume" under the gate electrode, "is below the channel of transistor 100 when conducting," see Blake at col. 5, lines 59-60. This means that Blake teaches the "body node" is actually separated from any gate electrode and gate electrode capacitance by at least the channel. See the "depletion regions" of Figs. 35 and 36 from pages 203 and 204 of Sze, SEMICONDUCTOR DEVICES, Physics and Technology, 1985, attached hereto. Just as gate capacitance between a gate and the substrate surface it is separated from by a gate oxide is not a capacitance "in the body link or recessed region 20" of Chen, it is also not a capacitance in the "body node" of Blake.

The Examiner further errs by urging that Gunning is relevant. However, Gunning is a reference concerned with "drivers and receivers for interfacing CMOS (complementary metal oxide semiconductor) digital circuits to transmission lines and, more particularly to relatively low power drivers and relatively sensitive receivers for interfacing VSLI (very large scale integrated) CMOS circuits to relatively low impedance, terminated transmission lines" as noted at col. 1, line 6-12. Where is the Roufett required reasonable explanation of the reasons why one of ordinary skill in the art would have been motivated to select Gunning and Chen and to attempt to combine their disparate teachings along with those of the other

references? Is the Examiner suggesting that the col. 7, lines 4-11 description of the Fig. 4 VLSI CMOS transmission line GTL driver would be reasonably considered to be the same as the Chen SOI CMOS integrated circuit?

Once again, it appears that subjective conjecture is being substituted for evidence in terms of unreasonably lifting unrelated reference teachings from disparate references and then augmenting them in an irrational manner using the present claims as a guide.

However, the question is what the references themselves reasonably suggest. In this regard, it is the burden of the PTO to demonstrate a *prima facie* case of obviousness which means the PTO must show that the relied upon references teach all of the limitations of the claims without resort to speculation to fill gaps missing from reference teachings as noted above relative to In re Warner.

Furthermore, the response filed March 20, 2001, noted the following:

> In addition to lacking any evidence that the artisan would have some reason to consider the product of the resistance value R of a fixed potential transmission path extending from a body contact to a body region of the nature claimed and the capacitance value C of a gate of an MOS transistor formed on an oxide film over the body region to be important to control, the Action further lacks any evidence that the artisan would have a prior art based reason to believe that this RC product having an R value and a C value from different elements is somehow a measure of how quickly the signal decays as stated at the top of page 3 of the Action. Similarly lacking is some prior art based reason to believe that this particular RC product having an R value determined by an interior body region and a C value related to a gate electrode over an oxide layer of transistor should be minimized as to a clock signal period so as to produce some desired result. As noted by In re Sporck, 133 USPQ 360, 364 (CCPA 1962):
>
> > Obviousness is a legal conclusion which we ware required to draw from facts appearing in the record or of which judicial notice may be taken. Thus before we can conclude that any disclosed invention is 'obvious' under the conditions specified in 35 U.S.C. §103, we must evaluate facts from which to

> determine (1) what was shown in the prior art at the time the invention was made, and (2) the knowledge which a person of ordinary skill in the art possessed at the time the invention was made. Here, neither the record nor the facts of which we are able to take judicial notice supplies the factual data necessary to support the legal conclusion of obviousness of the invention at the time it was made. We are unwilling to substitute speculation and hindsight appraisal of the prior art for such factual data.

B. Claims 2 and 4

With specific regard to Claim 2 and 4, the discussion starting at the bottom of page 5 and continuing through the top of page 8 of the response filed March 20, 2001, is again believed to be relevant and is repeated here for the Board's convenience as follows:

> Turning to Claim 2, it is again noted that this claim is similar to Claim 1 as to the method of designing that is recited and the semiconductor device to be designed. The differences relate to the requirements of Claim 2 that relate to a signal propagation delay time being provided instead of the Claim 1 operating frequency and the determining of the layout pattern being based on this signal propagation delay time instead of the Claim 1 operating frequency. In this regard, Claim 2 requires the layout pattern to be determined so that $(R \cdot C) / td < 1$ with the definitions of R and C being the same for Claim 2 as for Claim 1 and "td" being the signal propagation delay time of the MOS transistor which must be less than or equal to 50 ps.
>
> Once again relative to Claim 2, it is believed to be clear that if the artisan where to reasonably use the teachings of Agari and Chen to design the device of Iwamatsu, he would merely add a step as to determining an optimum wiring line width and spacing to result in minimizing RC delay as to the wiring lines shown in the upper portion of Fig. 1 of Iwamatsu as taught by Agari and a separate doping step to dope body links between body contacts and MOS transistors so that these body links themselves have a body link RC time constant as short as or less than 1 nsec. This is not the method set forth by Claim 2.
>
> Similarly, with respect to independent Claim 2, the teachings of Agari cannot be based upon extracting terms out of context and assigning meanings thereto that are not consistent with the meanings clearly used by Agari. See again the Wesslau decision discussed above. The rejection of Claim 2 is also

traversed as relying upon an improper interpretation of the language "wiring part" used by Agari just as the rejection of Claim 1 was.

Moreover, and as noted above, even if Agari is assumed to somehow teach minimizing the RC time constant of a body contact, the body contact of Chen is just that, not any of the doped body links disclosed to be between body contacts and MOS transistors also taught by Chen. What Claim 2 requires, on the other hand, is the use of a layout pattern to form an MOS transistor on an SOI layer that will satisfy the conditional expression (R·C) / td > 1 where C = the gate capacitance of said MOS transistor, R = the resistance of a fixed potential transmission path extending from said at least one body contact to said body region, and td = signal propagation delay time required for the MOS transistor, with td being less than or equal to 50 ps. None of Iwamatsu, Agari, or Chen teach any reason at all to consider multiplying the resistance value R of a fixed potential transmission path extending from a body contact to a body region of the nature claimed by the capacitance value C of a gate of an MOS transistor formed on an oxide film over the body region and multiplying the result by a signal propagation delay time td required for the MOS transistor, with td being less than or equal to 50 ps and insuring that the final result is less than one.

Clearly, the resistance "R" of concern in Claim 2 is again that of a "fixed potential transmission path" extending from a body contact to a body region as discussed above and not the resistance of the wiring line of concern to Agari. In addition none of Iwamatsu, Agari, or Chen teach any reason to use the capacitance "C" of the MOS transistor gate electrode along with this value R of an internal transmission path to form an RC product, much less one that meets the Claim 2 requirement that (R·C) / td <1 with td being less than or equal to 50 ps. Once again, valid rejections can only be made if they are based upon established facts as to the prior art. The rejection of Claim 2 is also traversed because speculation and hindsight based upon applicants' disclosure have again been used as a substitute for facts not of record.

Once again, the addition of Blake, Gunning and Masuda changes none of these points and cures none of the deficiencies noted as to Agari Chen, pr Iwamatsu. Consequently, the rejection of Claims 2 and 4 should be reversed for the reasons noted above as to the deficiencies of all of the relied upon references.

C. Claims 5 and 18

Claims 5 and 18 are specific to a semiconductor device having a particular resistance for the fixed potential transmission path primarily determined by body region 14 resistance defined in part by the thickness of the SOI layer times the length of the fixed potential transmission path along the gate length of the gate electrode. The various Office Actions of record, including the latest FR, have not set forth any attempt to establish a *prima facie* case of obviousness that addresses these limitations. Without such a *prima facie* case of obviousness, reversal is mandatory. See In re Fine, 5 USPQ2d 1596, 1598-99 (Fed. Cir. 1988).

Consequently, the rejection of Claims 5 and 18 should be reversed for the reasons noted above.

Appln. No.: 09/176,315
Docket No. 0057-2362-2YY

CONCLUSION

The rejection as applied to Claims 1-5 and 18 should be reversed for the above-noted reasons.

Respectfully submitted,

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APPENDIX

1. A method of designing a semiconductor device including a MOS transistor formed on an SOI substrate including a supporting substrate, a buried oxide film and an SOI layer, said MOS transistor being operated based on a predetermined clock,

said MOS transistor comprising:

a first semiconductor region of a first conductivity type and selectively formed in said SOI layer;

a second semiconductor region of said first conductivity type and selectively formed in said SOI layer independently of said first semiconductor region;

a body portion of a second conductivity type and including a body region, said body region being a region of said SOI layer which lies between said first and second semiconductor regions;

a gate electrode formed on a gate oxide film formed on said body region; and

at least one body contact electrically connected to said body portion and receiving a fixed potential,

said method comprising the steps of:

(a) providing an operating frequency of said predetermined clock; and

(b) determining a layout pattern of said MOS transistor based on the operating frequency of said predetermined clock,

wherein the layout pattern of said MOS transistor is determined in said step (b) so as to satisfy the conditional expression

$$R \cdot C \cdot f < 1$$

where

C = the gate capacitance said MOS transistor,

R = the resistance of a fixed potential transmission path extending from said at least one body contact to said body region,

f = the operating frequency of said predetermined clock, and

$f \geqq 500$ MHZ.

2. A method of designing a semiconductor device including a MOS transistor formed on an SOI substrate including a supporting substrate, a buried oxide film and an SOI layer,

said MOS transistor comprising:

a first semiconductor region of a first conductivity type and selectively formed in said SOI layer;

a second semiconductor region of said first conductivity type and selectively formed in said SOI layer independently of said first semiconductor region;

a body portion of a second conductivity type and including a body region, said body region being a region of said SOI layer which lies between said first and second semiconductor regions;

a gate electrode formed on a gate oxide film formed on said body region, said gate electrode being electrically connected to said body portion; and

at least one body contact electrically connected to said body portion and receiving a fixed potential,

said method comprising the steps of:

(a) providing a signal propagation delay time required for said MOS transistor; and

(b) determining a layout pattern of said MOS transistor based on said signal propagation delay time,

wherein the layout pattern of said MOS transistor is determined in said step (b) so as to satisfy the conditional expression

$(R \bullet C)/td < 1$

where

C = the gate capacitance of said MOS transistor,

R = the resistance of a fixed potential transmission path extending from said at least one body contact to said body region,

td = signal propagation delay time (s) required for said MOS transistor, and

$td \leqq 50$ ps.

3. A semiconductor device designed by the method as recited in claim 1.

4. A semiconductor device designed by the method as recited in claim 2.

5. The semiconductor device according to claim 3,

wherein said resistance R of said fixed potential transmission path is determined by

$R = (\rho \bullet W)/(L \bullet t_{SOI})$

where

W = the length of said fixed potential transmission path in said body region along the gate width of said gate electrode,

L = the length of said fixed potential transmission path in said body region along the gate length of said gate electrode,

t_{SOI} = the thickness of said SOI layer, and

ρ = the resistivity of said body region.

18. The semiconductor device according to claim 4,

wherein said resistance R of said fixed potential transmission path is a determined by

$R = (\rho \bullet W)/(L-t_{SOI})$ where

W = the length of said fixed potential transmission path in said body region along the gate width of said gate electrode,

L = the length of said fixed potential transmission path in said body region along the gate length of said gate electrode,

t_{SOI} = the thickness of said SOI layer, and

ρ = the resistivity of said body region.

ATTACHMENT

SEMICONDUCTOR DEVICES
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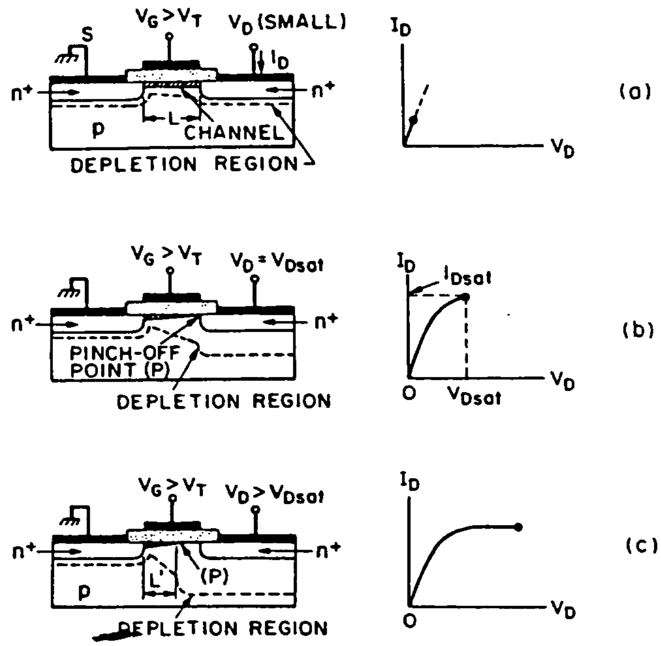

Fig. 35 Operations of the MOSFET and output *I–V* characteristics. (*a*) Low drain voltage. (*b*) Onset of saturation. Point P indicates the pinch-off point. (*c*) Beyond saturation.

tion is called the gradual-channel approximation and generally is valid for long-channel MOSFETs.

Figure 36*a* shows a MOSFET operated in the linear region. Under the above ideal conditions, the total charge induced in the semiconductor per unit area, Q_s, at a distance y from the source is shown in Fig. 36*b*, which is an enlarged central section of Fig. 36*a*. Q_s is given from Eqs. 65 and 66 by

$$Q_s(y) = -[V_G - \psi_s(y)]C_o \tag{77}$$

where $\psi_s(y)$ is the surface potential at y and $C_o = \epsilon_{ox}/d$ is the gate capacitance per unit area. The charge in the inversion layer is given by Eqs. 56 and 77:

$$\begin{aligned} Q_n(y) &= Q_s(y) - Q_{sc}(y) \\ &= -[V_G - \psi_s(y)]C_o - Q_{sc}(y)\,. \end{aligned} \tag{78}$$

The surface potential $\psi_s(y)$ at inversion can be approximated by $2\psi_B + V(y)$, where $V(y)$ as shown in Fig. 36*c* is the reverse bias between the point y and the source electrode (which is assumed to be grounded). The charge within the surface depletion region $Q_{sc}(y)$ was given previously as

$$Q_{sc}(y) = -qN_A W_m \simeq -\sqrt{2\epsilon_s q N_A[V(y) + 2\psi_B]}\,. \tag{79}$$

Substituting Eq. 79 in 78 yields

$$Q_n(y) \simeq -[V_G - V(y) - 2\psi_B]C_o + \sqrt{2\epsilon_s q N_A[V(y) + 2\psi_B]}\,. \quad (80)$$

The conductivity of the channel at position y can be approximated by

$$\sigma(x) = qn(x)\mu_n(x)\,. \quad (81)$$

For a constant mobility the channel conductance is then given by

$$g = \frac{Z}{L}\int_0^{x_i}\sigma(x)\,dx = \frac{Z\mu_n}{L}\int_0^{x_i} qn(x)\,dx\,. \quad (82)$$

The integral $\int_0^{x_i} qn(x)\,dx$ corresponds to the total charge per unit area in the inversion layer and is therefore equal to $|Q_n|$, or

$$g = \frac{Z\mu_n}{L}|Q_n|\,. \quad (83)$$

The channel resistance of an elemental section dy (Fig. 36*b*) is

$$dR = \frac{dy}{gL} = \frac{dy}{Z\mu_n|Q_n(y)|} \quad (84)$$

and the voltage drop across this elemental section is

$$dV = I_D\,dR = \frac{I_D\,dy}{Z\mu_n|Q_n(y)|} \quad (85)$$

where I_D is the drain current which is independent of y. Substituting Eq. 80 into Eq. 85 and integrating from the source ($y = 0$, $V = 0$) to the drain

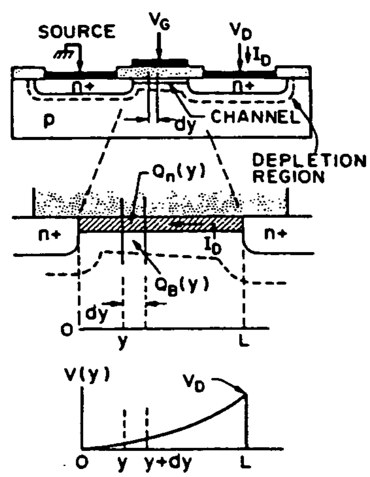

Fig. 36 (*a*) MOSFET operated in the linear region. (*b*) Enlarged view of the channel region. (*c*) Drain voltage drop along the channel.